REMARKS/ARGUMENTS

Claims 1-21 and 23-34 are pending. Claims 1, 21, 27, and 29 have been amended. No new matter has been added.

Claims 28 and 30 were rejected under 35 U.S.C. § 112, first paragraph. Applicant respectfully traverses the rejection. The paragraph starting on line 9 of page 7 of the specification has been amended to state that, "[t]he MgO layer is grown highly oriented on the amorphous gate oxide layer." The support for this is found in the article entitled, "Growth of highly oriented PB(Zr, Ti)O3 films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field -effect transistors (see the first paragraph on page. 3942)." This article was authored by the present inventor and published in Applied Physics Letters, Vol. 73, No. 26, and was filed as an Appendix to U.S. Provisional Application No. 60/173,175, filed on December 27, 1999, to which the present application claims priority. The provisional application also incorporates by reference this article (see page 5, second paragraph) . Copies of the transmittal page of the provisional application and the article are enclosed.

Claims 21, 23, 24, and 26-28 were rejected under 35 U.S.C. § 112, second paragraph. Applicant traverses the rejection. Claim 21 has been amended in response to the rejection.

Claims 1, 3-10, 14-18, 20, 21, 23, 24, and 27 were rejected under section 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirlin, Maiti, and Ilyer. Applicant respectfully traverses the rejection.

Claim 1 is directed to a method for fabricating a non-volatile memory device. The claim recites, "...forming an oxide layer on the silicon substrate, the oxide layer having an amorphous surface structure; forming a buffer layer on the amorphous oxide layer after forming the oxide layer over the substrate, the buffer layer having a crystalline structure; thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer; forming a ferroelectric material overlying the substrate and on the buffer layer..."

The claimed invention relates to using a ferroelectric material, e.g., PZT bearing compound, to form a transistor. A conventional gate oxide formed on the silicon substrate is

used in the claimed invention since a gate oxide formed directly onto the silicon substrate generally provides superior characteristics than that formed indirectly onto the silicon substrate, i.e., the gate oxide is grown between a silicon substrate and another layer. Accordingly, the claimed invention provides the benefit of using both a ferroelectric material and a convention gate oxide formed directly on the silicon substrate.

Hirai discloses a method of forming a transistor using a ferroelectric film and a paraelectric oxide film. The paraelectric oxide film provides a template whereon the ferroelectric film is grown. The paraelectric oxide itself is grown on an oriented template, e.g., a silicon substrate. A silicon oxide layer, which is amorphous, is provided between the paraelectric oxide film and the silicon substrate after the oriented paraelectric oxide film has been formed. Hirai has opted for the above method that does not use a silicon oxide layer (or gate oxide layer) that has been formed directly onto the silicon. Rather it uses an inferior gate oxide layer, i.e., a silicon oxide layer that is formed after the paraelectric oxide film has been formed on the silicon substrate. This appears to be because Hirai is unaware of a technique for forming an oriented paraelectric oxide film on an amorphous silicon oxide layer. Therefore, Hirai does not disclose the above recited features of claim 1.

Hirai also does not disclose, "thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer; forming a ferroelectric material overlying the substrate and on the buffer layer." Hirai does not disclose or suggest a need for such an annealing process to enhance the crystal alignment. This is because Hirai discloses formation of the paraelectric oxide film on a silicon substrate having a crystal structure.

The Examiner argues that the annealing step of MgO layer is disclosed in each of Maiti and Kirin to remove oxygen vacancies (see Maiti, col. 3:33-35; Kirin, col. 35:28-33). Applicant does not believe these annealing steps are equivalent to the annealing step recited in claim 1, i.e., to enhance the crystal alignment.

More importantly, there is no motivation to combine Hirai to Maiti or Kirlin. Hirai does not disclose or suggest the annealing step to enhance the crystal alignment of the MgO layer. This motivation is based on the teaching of the claimed invention, i.e., based on inappropriate hindsight.

It is well settled law that one cannot use hindsight to reconstruct the claimed invention by picking and choosing features from prior art. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification...It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."" *In re Fritch*, 23 USPQ 2d 1780, 1783-84, (Fed. Cir. 1992).

As the Examiner noted that Hirai discloses forming an silicon oxide layer 4 directly on a silicon substrate 1 and then forming a paraelectric oxide thin film 5 on the silicon oxide film 4 (col. 8:1-9). However, Hirai does not disclose how a buffer layer, e.g., MgO layer, having a crystalline structure is formed on the amorphous silicon oxide layer. Those skilled in the art have believed that this was not possible until the present inventor's discovery, as documented by the inventor's article published in Applied Physics Letters, Vol. 73 , No. 26.

In fact, Hirai provides elsewhere extensive details about forming the paraelectric oxide thin film 5 on the silicon substrate, apparently because its inventors do not believed that an oriented paraelectric oxide film can be formed on an amorphous silicon oxide film.

Accordingly, the brief description above in Hirai merely appears to be an "invitation to explore," rather than a meaningful disclosure/teaching. An invention is not made obvious by a statement or guidance "that provides only general guidance and is not at all specific as to the particular form of the claimed invention and how to achieve it." *Ex parte Obukowicz*, 37 USPQ 2d 1063, 1065 (B.P.A.I. 1992). For the reasons set forth above, claim 1 is allowable.

Claim 21 recites, "...forming a MgO layer overlying on the oxide layer after forming the oxide layer on the substrate, the MgO layer having a crystal structure; thermally annealing the second buffer layer MgO layer to enhance an alignment of crystallites of the second buffer MgO layer..." Hirai does not disclose or suggest these features. Other references do not remedy the deficiency of Hirai. Claim 21 is allowable at least for this reason.

Other claims depend from either claim 1 or 21 and are allowable at least for this reason.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Yamazaki. Applicant respectfully traverses the rejection. Claim 2 depends from claim 1 and is allowable at least for this reason.

Claims 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Van Zant and Evetts. Applicant respectfully traverses the rejection. Claims 11 and 12 depend from claim 1 and are allowable at least for these reasons.

Claim13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts and Wolf. Applicant respectfully traverses the rejection. Claim 13 depends from claim 1 and is allowable at least for this reason.

Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Jaeger. Applicants respectfully traverses the rejection. Claim 19 depends from claim 1 and is allowable at least for this reason.

Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Wolf. Applicant respectfully traverses the rejection. Claim 26 depends from claim 21 and is allowable at least for this reason.

Claims 29 and 31-33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai and Iyer. Applicant respectfully traverses the rejection. Claim 29 recites, "forming an oxide layer on the substrate, the oxide layer having a non-crystalline structure; forming a MgO layer on the oxide layer, the MgO layer formed on the oxide layer having a highly-oriented structure..." The cited references do not disclose or suggest the above recited features. Claim 29 is allowable at least for this reason.

Claim 32 recites, "forming an amorphous gate dielectric layer on the substrate; forming a MgO layer on the amorphous dielectric layer after forming the dielectric layer on the substrate, the MgO layer having a highly-oriented structure..." The cited references do not disclose or suggest the above recited features. Claim 32 is allowable at least for this reason. Other claims depend from claim 29 or 32 and are allowable at least for this reason.

Claim 30 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Iyer in view of Kirlin and Maiti. Applicant respectfully traverses the rejection. Claim 30 depends from claim 29 and is allowable at least for this reason.

Claim 34 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai/Iyer in view of admitted prior art. Claim 33 depends from claim 32 and is allowable at least for that reason.

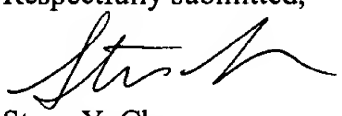
Applicant respectfully requests the Examiner for a telephone interview prior to issuing a next Office Action, unless it is a Notice of Allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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